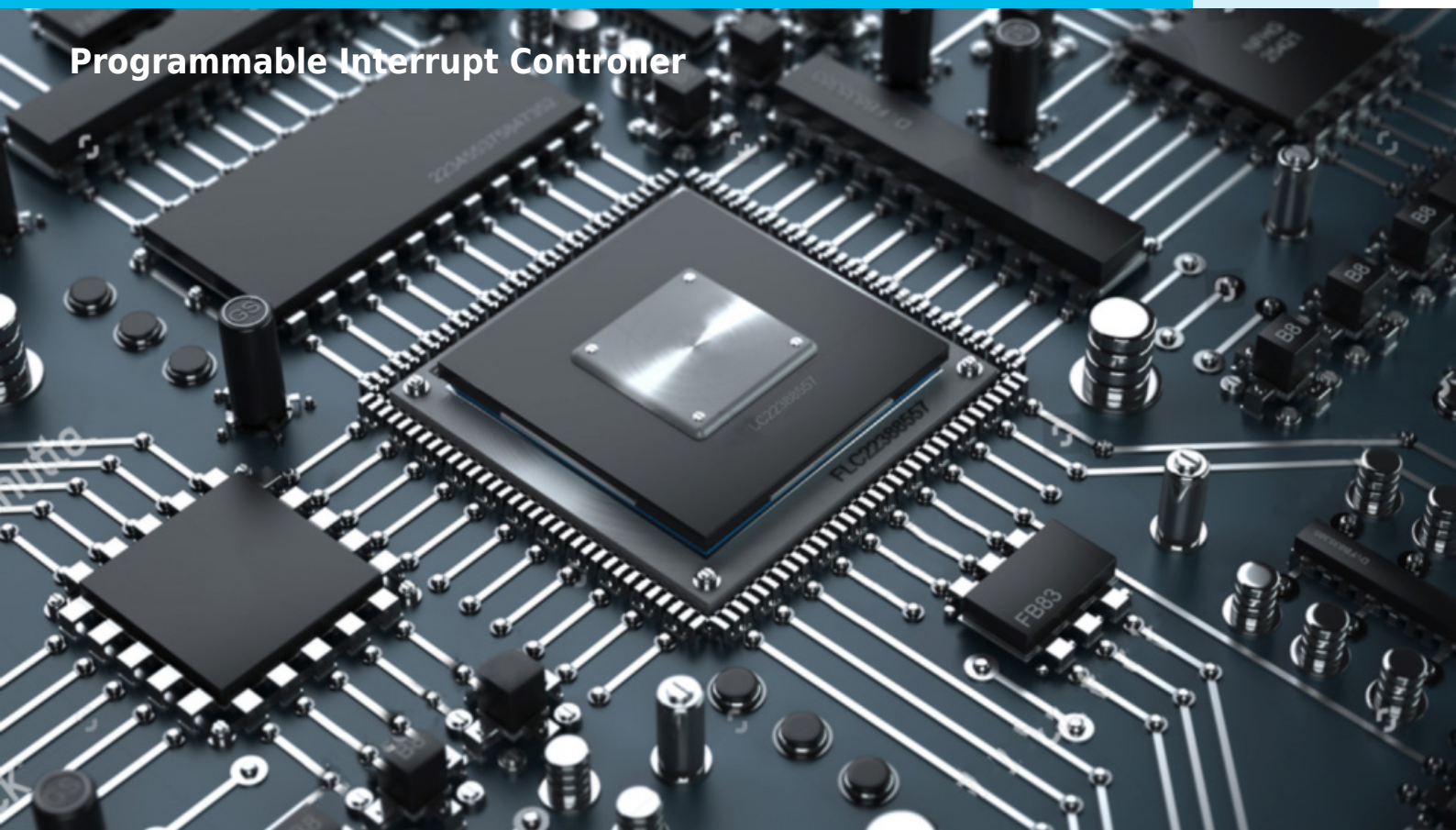
D8259

Programmable Interrupt Controller



COMPANY OVERVIEW

DCD-SEMI is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D8259 is a soft Core of **Programmable Interrupt Controller**, **fully compatible with the 82C59A device**. Our efficient IP core can manage **up to 8-vectored priority interrupts** for the processor. Moreover, you can also program it to cascade and gain up to **64 vectored interrupts**. And if it's not enough, you can always get more than 64 vectored interrupts. Just program our IP Core to the **Poll Command Mode**. The D8259 can operate in all 82C59A modes and supports all 82C59A features. The D8259 Package includes **fully automated test bench**. Thanks to **complete set of tests** you can easily validate the whole package at each stage of SoC design flow. Same as all DCD's IP Cores, this one's also got technology independent design which can be implemented in a variety of process technologies.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

KEY FEATURES

- 8 vectored priority interrupts
- Up to sixty-four vectored priority interrupts with cascading
- Support for all 82C59A modes features
  - MCS-80/85 and 8088/8086 processor modes
  - Fully nested mode and special fully nested mode
  - Special mask mode
  - Buffered mode
  - Pool command mode
  - Cascade mode with master or slave selection
  - Automatic end-of-interrupt mode
  - Specific and non-specific end-of-interrupt commands
  - Automatic and Specific Rotation
  - Edge and level triggered interrupt input modes
  - Reading of interrupt request register (IIR) and in-service register (ISR) through data bus
- Fully synthesizable HDL Source Code
- Static design and no internal tri-states

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use
- All latches implemented in original 8255 devices are replaced by equivalent flip-flop registers, with the same functionality

UNITS SUMMARY

Data Bus Buffer – The Data Bus Buffer is used to interface the D8255, to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions, by the CPU. Control words and status information are also transferred through the data bus buffer.
Read/Write and Control Logic – The control logic block manages all of the internal and external transfers of both, Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both, A and B Control Groups.
Ports A, B, and C – The D8255 contains three 8-bit ports. All can be configured in a wide variety of functional characteristics by the system software, but each has its own special features or "personality", for further enhancement of the power and flexibility of the D8255.
Port A – One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both „pull-up" and "pulldown" bus hold devices present on Port A.
Port B – One 8-bit data input/output latch/buffer. Only „pull-up" bus hold devices are present on Port B.
Port C – One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs and status signal inputs, in conjunction with ports A and B. Only „pull-up" bus hold devices are present on Port C.
Group A and Group B Controls – The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the D8255. The control word contains information, such as "mode"', "bit set", "bit reset", etc., that initializes the functional configuration of the D8255. Each of the Control blocks (Group A and Group B), accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.
Group A – Port A and upper half of Port C
Group B – Port B and lower half of Port C

The control word register can be both written and read. The figure on the right shows the control word format, for both Read and Write operations. When the control word is read, bit D7 will always be logic “1”, as this implies control word mode information.

APPLICATIONS

- Embedded microprocessor boards

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PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	F_{max}
CYCLONE V	210	154 MHz
CYCLONE IV	403	189 MHz
CYCLONE III	409	186 MHz
CYCLONE 2	387	163 MHz
CYCLONE	394	154 MHz
ARRIA V	213	336 MHz
ARRIA II	341	316 MHz
STRATIX V	213	357 MHz
STRATIX IV	331	347 MHz
STRATIX III	344	365 MHz
STRATIX II	294	239 MHz
MAX V	405	54 MHz
MAX II	405	107 MHz

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– Verilog or VHDL RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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