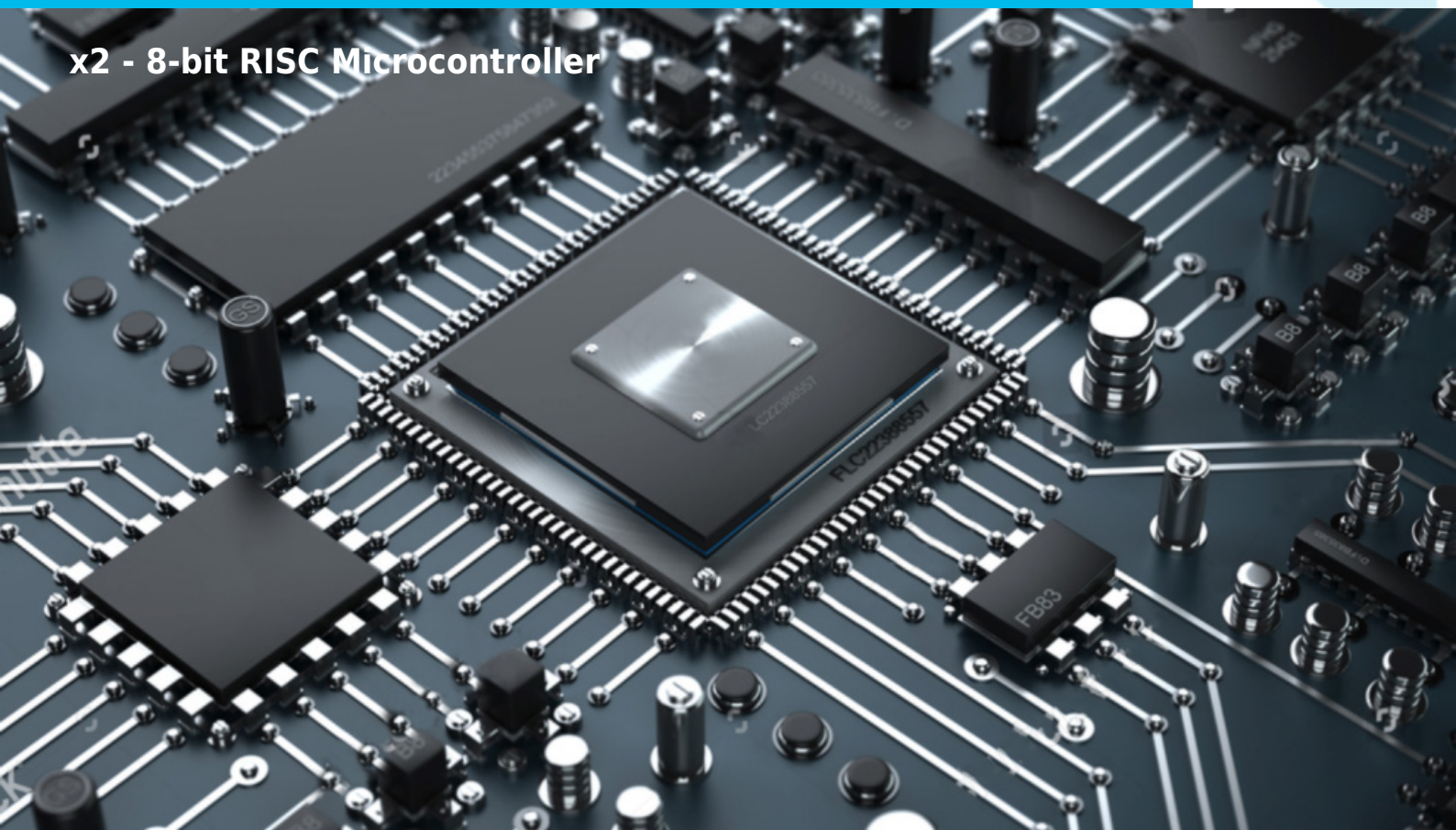
DFPIC165X



COMPANY OVERVIEW

DCD-SEMI is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DFPIC165X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated to operate with **fast memory** (typically on-chip). The core is designed with a special concern about **low power consumption**. The DFPIC165X is software compatible with PIC16C54, PIC16C55, PIC16C56, PIC16C57 and PIC16C58 industry standards. It contains modified RISC architecture (2 times faster than original implementation). The DFPIC165X have enhanced core features and configurable hardware stack. Separate instruction and data buses allow a 12 bit wide instruction word, with a separate 8 -bit wide data. The DFPIC165X typically achieves a 2:1 code compression and an 8:1 speed improvement over other 8-bit microcontrollers in its class. The Core has 24 I/O lines and an 8-bit timer/counter with an 8-bit programmable prescaler. The power-down SLEEP mode allows user to reduce power consumption. The user can wake the controller up from the SLEEP mode through a user reset or a watchdog overflow. An integrated Watchdog Timer with its own clock signal provides protection against software lock-up. The DFPIC165X Microcontroller fits well in applications ranging from high-speed automotive and appliance motor control, to low-power remote transmitters/receivers, pointing devices and telecom processors. A built-in power save mode and a small used area in programmable devices, make this IP perfect for applications with space and power consumption limitations. The DFPIC165X is delivered with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

Each of DCD's PIC Cores has a built-in support for a proprietary Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger** which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides non-intrusive debugging of a running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, SFRs, user defined peripherals, data and program memories.

CPU FEATURES

- Software compatible with industry standard PIC16C5X
- Harvard RISC architecture
- 2 times faster, compared to original implementation
- 33 instructions
- 12 bit wide instruction word
- Up to 256 bytes of internal Data Memory
- Up to 4K bytes of Program Memory
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Technology independent HDL Source Code
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

- **Three 8 bit I/O ports**
  - Three 8-bit corresponding TRIS registers
- **Timer 0**
  - 8-bit timer/counter
  - Readable and Writable
  - 8-bit software programmable prescaler
  - Internal or external clock select
  - Edge select for external clock
- **Watchdog Timer**
  - Configurable Time out period
  - 7-bit software programmable prescaler
  - Dedicated independent Watchdog Clock input

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DFPIC165X Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **Full duplex UART**
- **SPI – Master and Slave Serial Peripheral Interface**
- **I2C bus controller – Master**
- **I2C bus controller – Slave**

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs arithmetic and logic operations, during execution of an instruction. This module contains work register (W) and Status register.
Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.
Hardware Stack – The DFPIC165X configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack, when CALL instruction is executed or an interrupt causes a branch. The stack is popped during RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed two times, the third push overwrites the value that was stored from the first push.
RAM Controller – It performs interface functions between Data memory and DFPIC165X internal logic. It assures correct

Data memory addressing and data transfers. The DFPIC165X supports two addressing modes: direct or indirect. In Direct Addressing, the 8-bit direct address is computed from FSR(7:5) bits and from 5 least significant bits of instruction word. Indirect addressing is possible, by using the INDF register. Any instruction using INDF register, actually accesses data pointed to by FSR (file select register). Reading INDF register indirectly, will produce 00h. Writing to the INDF register indirectly, results in a no-operation. An effective 8-bit address is obtained from an 8-bit FSR register.

Timer 0 – Main system's timer and prescaler. The DFPIC165X Timer operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer registers are incremented every 4 CLK periods. When the prescaler is assigned into the TIMER pre-scale ratio can be divided by 2, 4 .. 256. In the "counter mode", the timer register is incremented every falling or rising edge of T0CKI pin, depending on T0SE bit in OPTION register.

Watchdog Timer – it is a free running timer. WDT has own clock input, separate from system clock. It means, that the WDT will run even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode, the WDT timeout causes the device to wake up and continue with normal operation.

I/O Ports – Block contains DFPIC165X's general purpose I/O ports and data direction registers (TRIS). The DFPIC165X has three 8-bit full bi-directional ports PORT A, PORT B and PORT C. Read and write accesses to the I/O port are performed via their corresponding SFR's PORTA, PORTB, PORTC. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has a corresponding bit in TRISA, TRISB and TRISC registers. When the bit of TRIS register is set, this means that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

CONFIGURATION

The following parameters of the DFPIC165X core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

– RAM memory type: *synchronous / asynchronous*
– RAM size: *up to 256 / default 128*
– Program Memory size: *up 4 kWords / default 2k*
– Number of hardware stack levels: *1-8 / default 2*
– SLEEP mode: *used / unused*
– WATCHDOG Timer: *used/width / unused*
– Timer system: *used / unused*
– PORTS A,B,C: *used / unused*

IMPROVEMENT

Most instruction of DFPIC165X is executed within 2 CLK cycles. Except the conditional program memory branches, in case the condition of branch instruction is met. The following table shows sample instructions execution times.

Mnemonic operands	DFPIC165X (CLK cycles)	PIC16C54 (CLK cycles)	Impr.
ADDWF	2	4	2
ANDWF	2	4	2
RLF	2	4	2
BCF	2	4	2
DECFSZ	2(4)[1]	4(8)[1]	2
INCFSZ	2(4)[1]	4(8)[1]	2
BTFSC	2(4)[1]	4(8)[1]	2
BTFSS	2(4)[1]	4(8)[1]	2
CALL	2	8	4
GOTO	2	8	4
RETLW	2	8	4

[1]– number of clock in case that result of operation is 0.

PERFORMANCE

The following table gives a survey about the Core area and performance in **XILINX®** devices after Place & Route:

Device	Speed grade	Slices	F_{max}
VIRTEX-IV	-12	285	90 MHz
VIRTEX-IIP	-7	270	106 MHz
VIRTEX-II	-6	270	84 MHz
VIRTEX-E	-8	266	56 MHz
VIRTEX	-6	266	44 MHz
SPARTAN-IIIE	-4	284	42 MHz
SPARTAN-III	-5	271	58 MHz
SPARTAN-IIE	-7	266	49 MHz
SPARTAN-II	-6	266	48 MHz

*CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, 256 B RAM, 4k of Program memory.

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation

- 12 months maintenance
  - Delivery of the IP Core and documentation updates
  - Phone & email support
  - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– Verilog or VHDL RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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