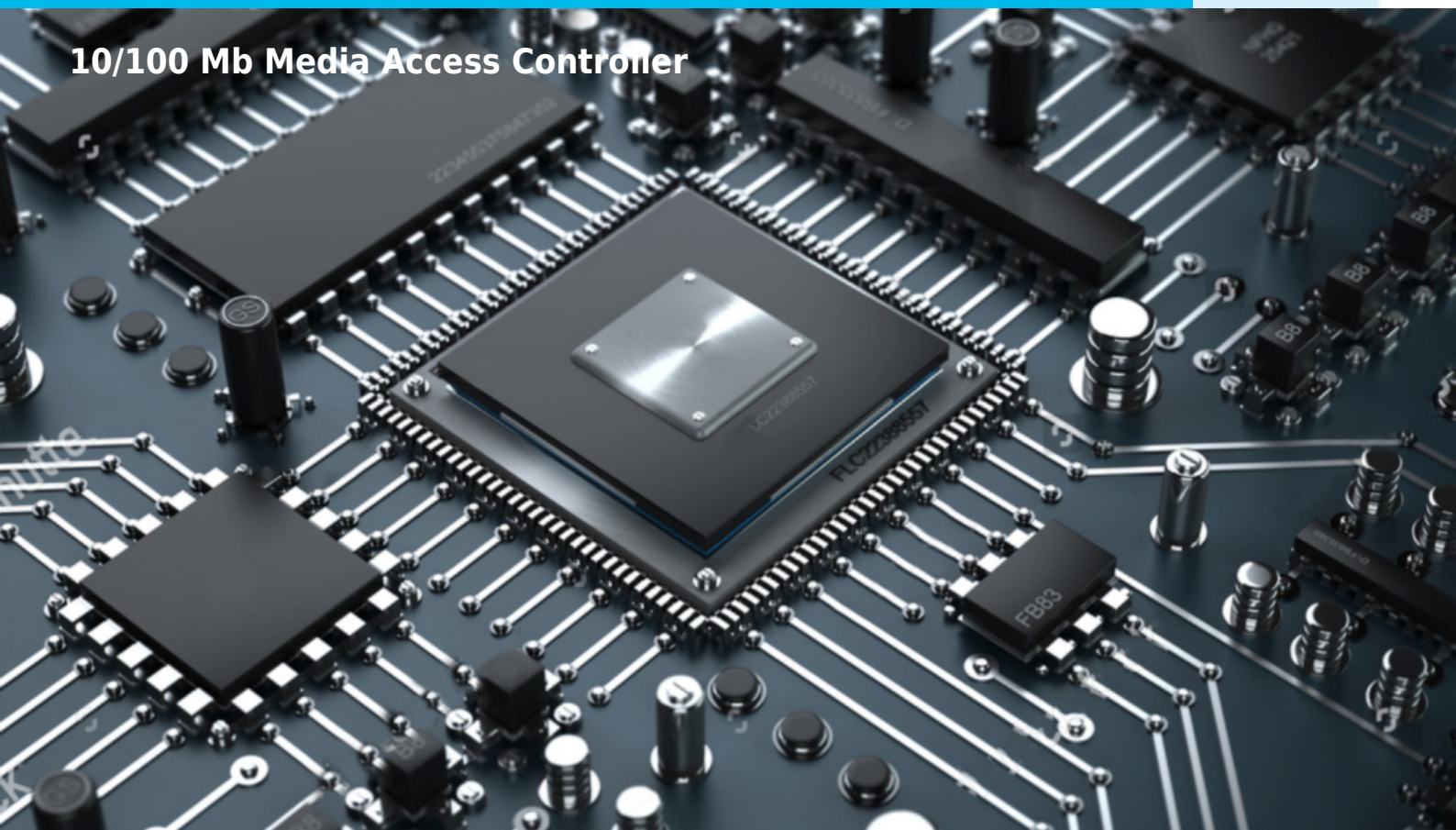
DMAC

10/100 Mb Media Access Controller



COMPANY OVERVIEW

DCD-SEMI is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DMAC bridge to APB, AHB, AXI bus. The Ethernet specification served as the basis for the 802.3 standard, which specifies the physical and lower software layers. Since its commercial release, Ethernet has retained a good degree of compatibility. DCD-SEMI **focuses on innovation** but remembers about standardization. That's why our **DMAC** solution is a **hardware implementation** of media access control protocol defined by the IEEE standard. Thanks to our IP Core, functionality in **design has never been better before**. The DMAC in cooperation with external PHY device enables network functionality in design. It is able to transmit and receive Ethernet frames to and from network. **Half and full duplex modes are supported**, as well as **10** and **100 Mbit/s speed**. The Core can work with **wide range of processors**: 8, 16 and 32 bit data bus, either little or big endian byte order format. The DMAC provides static configuration of PHY IC. Please remember that our design is technology independent, thus **can be implemented in variety of process technologies**. This Core strictly conforms to the **IEEE 802.3 standard**.

KEY FEATURES

- Conforms to IEEE 802.3-2002 specification
- Configurable width CPU interface with little or big endianess:
  - 8-bit
  - 16-bit
  - 32-bit
- Simple interface allows easy connection to CPU
- Narrow address bus (4 bits) with indirect I/O interface for transmitted and received data dual port memories
- Supports 10BASE-T and 100BASE-TX/FX IEEE 802.3 compliant MII PHYs
- Media Independent Interface (MII) for connection to external 10/100 Mbps PHY transceivers
- Supports full and half duplex operation at 10 Mbps or 100 Mbps
- CRC-32 algorithm:
  - calculates the FCS nibble at a time
  - automatic FCS generation and checking
  - able to capture frames with CRC errors if required
- Dynamic PHY configuration by STA management interface
- Early receive and transmit interrupts to increase data throughput
- Programmable MAC address
- Promiscuous mode support
- Allows operation from a wide range of input bus clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Lite Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

UNITS SUMMARY

Transmit module – Performs transmit management functions, sends frames to Ethernet medium.
Receive module – is responsible for receiving frames from the Ethernet. Provides necessary functions for frame decapsulation, CRC checking, address recognizing and error detection.
Synchronization logic – There are 3 clock domains in the DMAC core – this module performs synchronization between them.
TX RAM / RX FIFO RAM interfaces – Interfaces to external dual port memories used by the DMAC core, to store received and transmitted frames.
Control and I/O logic – This module provides interface to CPU/BUS. It exchanges data and control logic with transmit and receive modules, thus controls these, to perform transmit and receive operations.
STA – Station Management entity, enables communication with PHY, via simple serial management interface.

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

Component	Area	
	[gates]	[FFs]
RX	2200	172
RX FIFO	1100	131
TX	2400	197
Control & I/O logic	1500	202
STA	600	53
Total area	7800	755

Device	Speed	Min area	F_{max} [MHz] clk / txclk / rxclk
0.25 um	typical	7800 gates	250 / >50 / >50
0.18 um	typical	7800 gates	360 / >50 / >50
0.09 um	typical	6400 gates	800 / >50 / >50
0.06 um	typical	6300 gates	900 / >50 / >50

rxclk, txclk – design clock is 25 MHz

APPLICATIONS

- Embedded microprocessor boards
- Networking devices (Network Interface Cards, routers, switches)
- Communication systems

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– Verilog or VHDL RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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