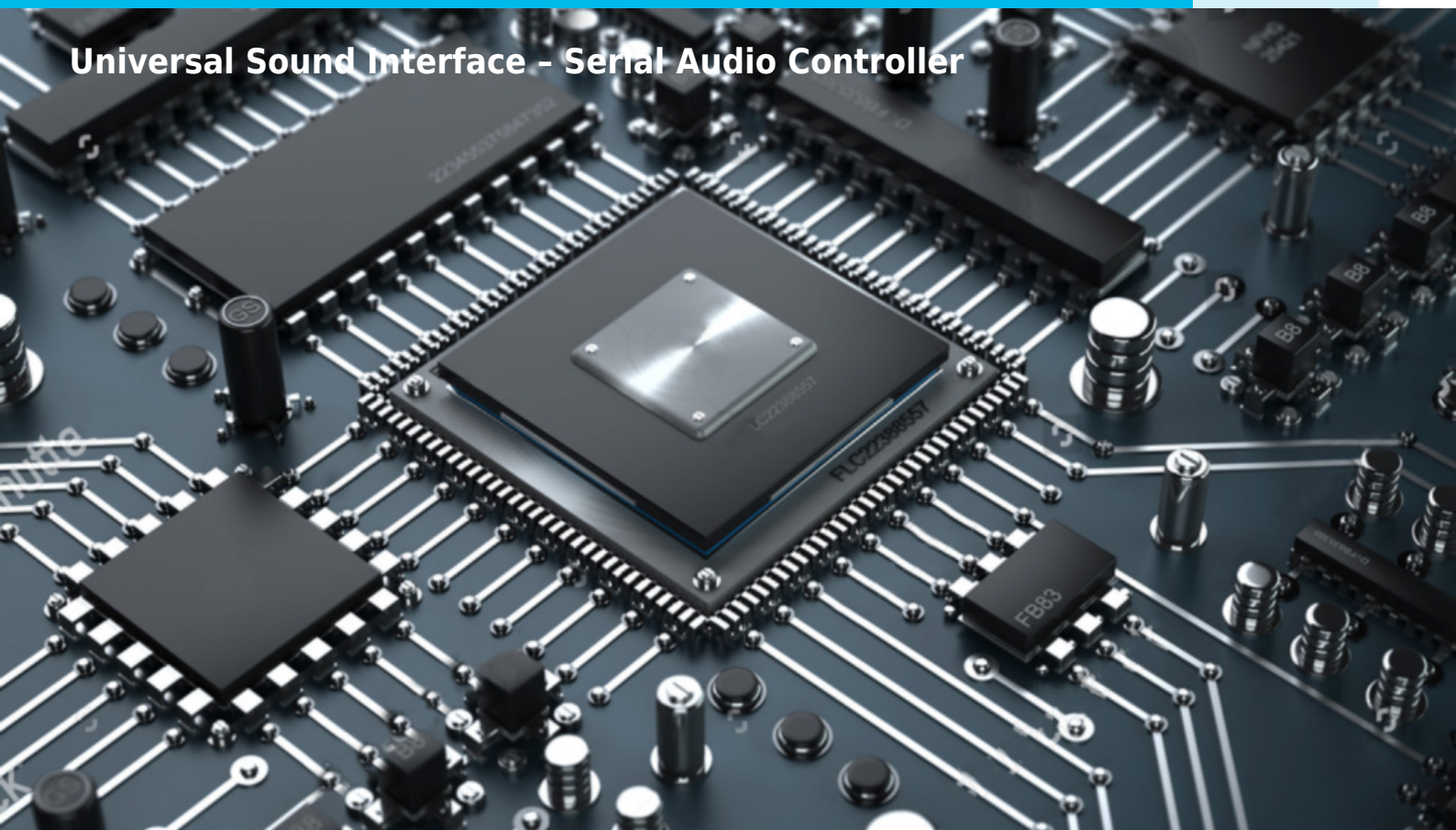
DI2S



COMPANY OVERVIEW

DCD-SEMI is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2S bridge to APB, AHB, AXI bus, it is a **universal solution** which provides an interface between a microprocessor and **I²S, left/right justified modes, PCM, TDM audio protocol codec**. Thanks to **flexible configuration** it can work as a **receiver**, **transmitter in master or slave mode**, with **configurable channel length** or **sample size**. Additionally, number of audio blocks can be adjusted according to specific project needs.

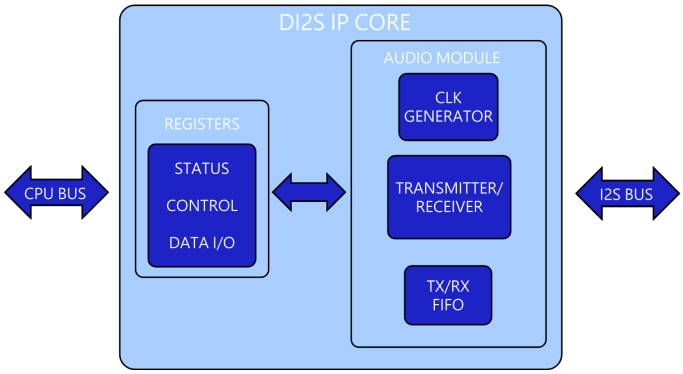
KEY FEATURES

- Configurable number of independent audio modules with their respective FIFO
- Configurable TX/RX mode of each audio module
- Configurable master/slave mode support of each audio module
- Flexible I2S, LSB/MSB (right/left) justified, DSP, TDM modes support
- Configurable sample size (8, 10, 16, 20, 24, 32 bit)
- Configurable number of samples per frame (1 to 16)
- Configurable FIFO depth
- Flexible FIFO threshold interrupt control
- FIFO Underrun/overrun interrupt
- Inter modules clock synchronization
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

DELIVERABLES

- Source code:
  - VERILOG Source Code
  - VERILOG test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
- Technical documentation
  - HDL core specification
  - Datasheet
- Technical support
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

BLOCK DIAGRAM



PERFORMANCE

In this section DI2S implementation results on **INTEL Cyclone V FPGA®** devices after Place & Route (all key features included):

Configuration type	ALUT	Registers
Single audio block	596	191
Double audio block	1250	386
Triple audio block	1728	559
Quad audio block	2214	698

Note that all results assume the most flexible audio block configuration and clocks synchronization, in many dedicated applications those results could be significantly reduced.

In this section DI2S implementation results on **INTEL Cyclone MAX 10 FPGA®** devices after Place & Route (all key features included):

Configuration type	LEs	Registers
Single audio block	611	189
Double audio block	1273	378
Triple audio block	1788	553
Quad audio block	2289	698

Note that all results assume the most flexible audio block configuration and clocks synchronization, in many dedicated applications those results could be significantly reduced.

LICENSING

Comprehensible and clearly defined licensing methods

without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

– VHDL or Verilog RTL synthesizable source code (called HDL Source code)

– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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