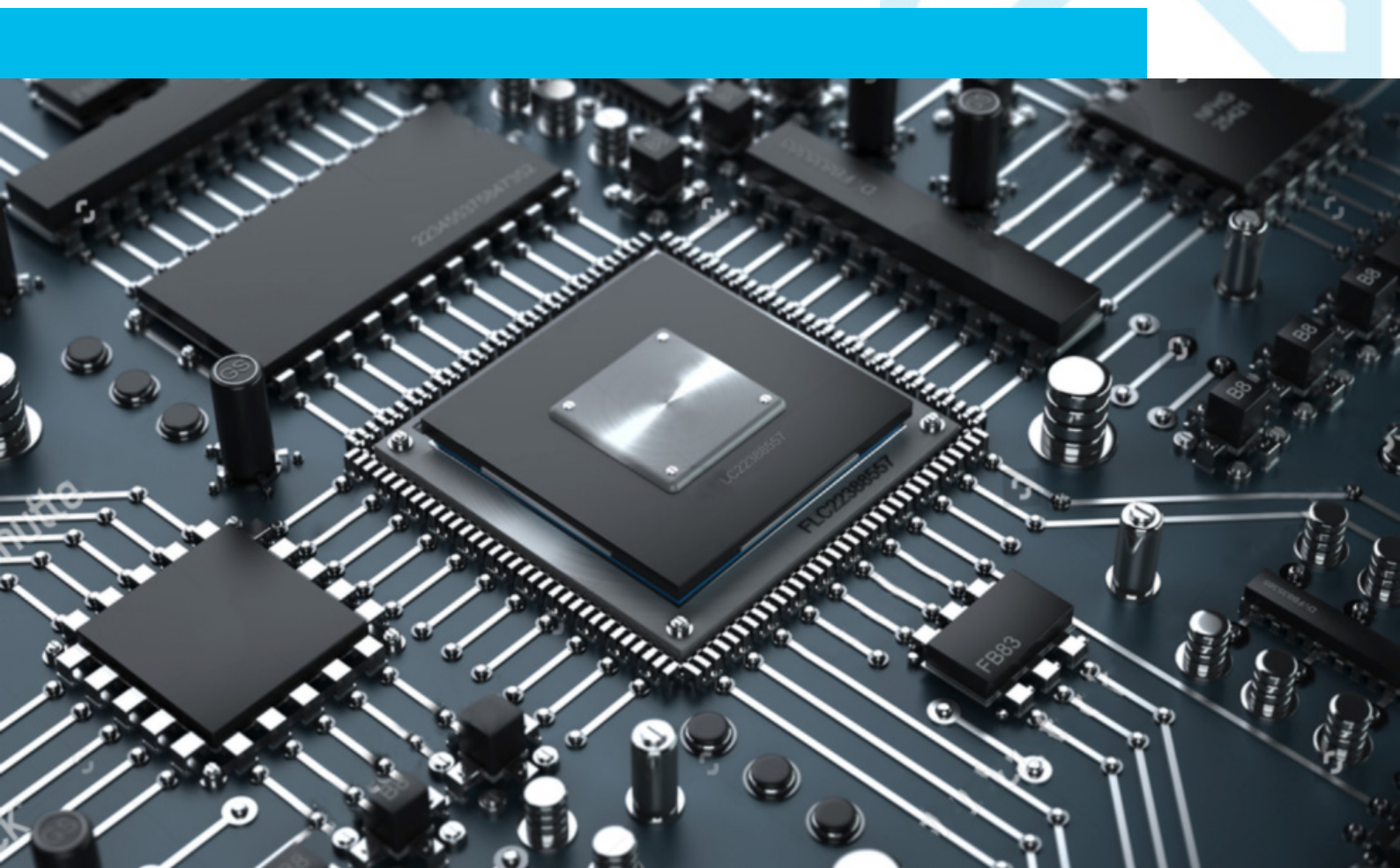




DOCD - DOWNLOAD AREA



COMPANY OVERVIEW

DCD-SEMI is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

Thank you for your continued interest in **DoCD™** debug software. The **DoCD™** supports all of the DCD's 8051/80251/80390 microcontrollers and DRPIC/DFPIC RISC. This is fully functional version of **DoCD™** debug software works in Simulator mode without any limitations. It is **free of charge** and granted to use in commercial and home applications. For more details about Licensing conditions, please read carefully **DoCD™** Software License Agreement.

To install the software please follow the instructions below:

- Download compressed file
- Unpack downloaded file into a temporary directory
- Run setup program and follow on screen instructions

8051/80251/80390 DoCD debugger

File name	Description
8051DoCD_Debug_v3.06a	DoCD™ 8051/80251/80390 complete package (unpacked, verified, signed, SHA-256, MD5, CRC32, and MD4)
8051DoCD.exe	DoCD™ 8051/80251/80390 executable
License	DoCD™ 8051/80251/80390 Software License Agreement
8051DoCD.exe	DoCD™ 8051/80251/80390 Debug Software with MD4 DF File - Application Note
8051DoCD.exe	DoCD™ 8051/80251/80390 Debugger with MD4 Unpacked/SHA256 - Application Note

DRPIC/DFPIC DoCD debugger

File name	Description
DRPIC_DoCD_v3.22	DoCD™ DRPIC/DFPIC complete package
DRPICDoCD.exe	DoCD™ DRPIC/DFPIC executable
License	DoCD™ DRPIC Software License Agreement
DRPICDoCD.exe	DoCD™ DRPIC/DFPIC Debug Software with MD4 Unpacked/SHA256 - Application Note

DF6811, DF6808, DF6805 DoCD debugger

File name	Description
DF6805_DoCD_v3.20	DoCD™ DF6805 complete package
DF6805DoCD.exe	DoCD™ DF6805 executable
License	DoCD™ Software License Agreement

GO BEYOND THE LIMITS

System-on-Chip designs are facing the problem of inaccessibility of important control and bus signals, because they often lay behind the physical pins of the device - that makes traditional measurement instrumentation useless. The best way to get around those limitations, is to use on-chip debug tools for the tasks verification and software debugging. Other advantage of an on-chip debugger, is its improved design productivity in an integrated environment, with graphical user's interface. Ability to display/modify memories' content, processor's and peripherals' register windows, along with information tracing and ability to see the related C/ASM source code, are the key elements, that help to improve the design process and thereby, to increase productivity.

INSTRUCTION SMART TRACE (IST)

The **DoCD™** Hardware Debugger provides debugging capability of a whole System on Chip (SoC). Unlike other on-chip debuggers, the DoCD™ provides non-intrusive debugging of a running application. It can also efficiently save designer's time, thanks to **hardware trace**, called **Instructions Smart Trace buffer (IST)**. The DoCD-IST **captures instructions in a smart and non-intrusive way**, so it doesn't capture addresses of all executed instructions, but only these related to the start of tracing, conditional jumps and interrupts. This method does not only **save time**, but also allows to **improve the size of the IST buffer and extend the trace history**. Captured instructions are read back by the DoCD-debug software, analyzed and then presented to the user as an ASM code and related C lines.

The screenshot displays a debugger interface with three main panels:

- Disassembled Source Code:** Shows assembly instructions for a function. Key instructions include:
 - 0x08C2 E4 CLR A
 - 0x08C3 FF MOV R7, A
 - 0x08C4 FE MOV R6, A
 - 0x08C5 90F800 MOV DPTR, 0x0F80
 - 0x08C8 ED MOVX A, @DPTR
 - 0x08C9 AB2A MOV R3, 0x2A
 - 0x08CB AA2B MOV R2, 0x2B
 - 0x08CD A92C MOV R1, 0x2C
 - 0x08CF 8F82 MOV DPL0, R7
 - 0x08D1 8E83 MOV DF0, R6
 - 0x08D3 120443 LCALL 0x0443
 - 0x08D6 0F INC R7
 - 0x08D7 BF0001 CJNE R7, #0x00
 - 0x08DA 0E INC R6
 - 0x08DB EF MOV A, R7
 - 0x08DC 7003 JNZ 0x08E1
 - 0x08DE EE MOV A, R6
 - 0x08E0 4402 JRL A, #0x02
 - 0x08E1 70E2 JNZ 0x08C5
 - 0x08E3 90F80F MOV DPTR, 0x0F80
 - 0x08E6 E0 MOVX A, @DPTR
 - 0x08E7 20E7F9 JB ACC.7, 0x08E4
 - 0x08EA C209 CLR 0x09
- Code Execution Trace:** Shows the execution of instructions with their addresses and values. Key entries include:
 - 0x08C5 90F800 MOV DPTR, 0x0F80
 - 0x08C8 ED MOVX A, @DPTR
 - 0x08C9 AB2A MOV R3, 0x2A
 - 0x08CB AA2B MOV R2, 0x2B
 - 0x08CD A92C MOV R1, 0x2C
 - 0x08CF 8F82 MOV DPL0, R7
 - 0x08D1 8E83 MOV DF0, R6
 - 0x08D3 120443 LCALL 0x0443
 - 0x08D6 0F INC R7
 - 0x08D7 BF0001 CJNE R7, #0x00, 0x08DB
 - 0x08DA 0E INC R6
 - 0x08DB EF MOV A, R7
 - 0x08DC 7003 JNZ A, R7, 0x08E1
 - 0x08DE EE MOV A, R6
 - 0x08E0 4402 JRL A, #0x02
 - 0x08E1 70E2 JNZ 0x08C5
 - 0x08E3 90F80F MOV DPTR, 0x0F80
 - 0x08E6 E0 MOVX A, @DPTR
 - 0x08E7 20E7F9 JB ACC.7, 0x08E4
 - 0x08EA C209 CLR 0x09
- Source Code - CF_FUNC.C:** Shows the C code corresponding to the assembly. Key lines include:
 - 282 buff2b[i] = cfv_dat;
 - 283 #else
 - 284 for(i=0;i<PHYSICAL_BLOCK_SIZE;i++) // read B data
 - 285 buff(i) = cfv_dat;
 - 286 #endif
 - 287 while(cfv_stat_comm & CF_BUSY); // wait for busy
 - 289 P10_MODEL = 0;
 - 290 P10_MODEL2 = 0;

PERFORMANCE

PERFECT SERVICE FOR FREE

The reason for the development of the **DoCD™**, was to provide our customers with the ability of easy system verification and software debugging, at no additional charges. Therefore, we have decided to add **the complete debug system** to each 8051/80251/80390 IP Core - **for free**

Now DCD's customers have the exceptional possibility, to obtain **the complete solution** for making their own 8051/80251/80390 based, SoC, with the ability to pre-silicon validation and post-silicon software debugging - **in one place**. It's really unusual opportunity for the designer, to have the ability to get a **high quality IP Core** and **unique on-chip debug tool**, from the same supplier.



customers which operate at several locations. The licensed product can be used at selected company branches. In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

- Verilog or VHDL RTL synthesizable source code (called HDL Source code)
- FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

- **Single-Site license option** - dedicated to small and middle sized companies which run their business at one place.
- **Multi-Site license option** - dedicated to corporate

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