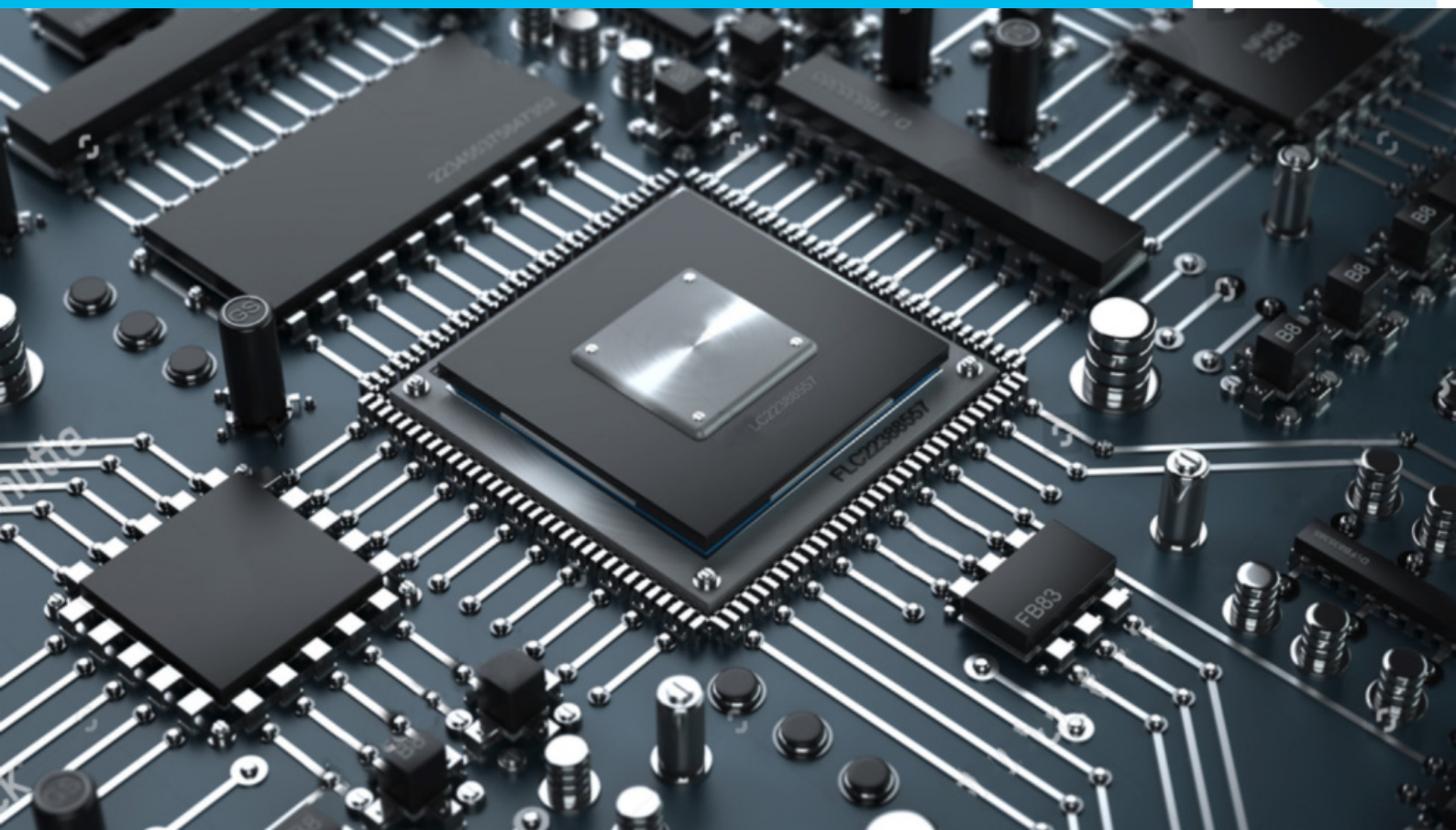
# DOCD – DOWNLOAD AREA



## COMPANY OVERVIEW

DCD-SEMI is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

## IP CORE OVERVIEW

Thank you for your continued interest in **DoCD™** debug software. The **DoCD™** supports all of the DCD's 8051/80251/80390 microcontrollers and DRPIC/DFPIC RISC. This is fully functional version of **DoCD™** debug software works in Simulator mode without any limitations. It is **free of charge** and granted to use in commercial and home applications. For more details about Licensing conditions, please read carefully **DoCD™** Software License Agreement.

### To install the software please follow the instructions below:

- Download compressed file
- Unpack downloaded file into a temporary directory
- Run setup program and follow on screen instructions

### 8051/80251/80390 DoCD debugger

| File name | Description |
|---|---|
| 8051/80251 DoCD v5.36A | DoCD™ 8051/80251/80390 complete package supporting certified Windows 7/8/8.1/10 x32/x64 HASP USB driver. |
| docd8.dp | DoCD™ 8051/80251/80390 datasheet |
| License | DoCD™ 8051/80251/80390/DoPIC Software License Agreement |
| docd_ba51 | Using DoCD™ 8051/80251/80390 Debug Software with Keil OMF files - Application Note |
| docd_ex51ba | Using DoCD™ 8051/80251/80390 debugger with Keil uVision2/3/4/5 - Application Note |

### DRPIC/DFPIC DoCD debugger

| File name | Description |
|---|---|
| DoPIC DoCD v2.22 | DoCD™ DRPIC/DFPIC complete package |
| PICdocd.dp | DoCD™ DRPIC/DFPIC datasheet |
| License | DoCD™ DoPIC Software License Agreement |
| DoPIC ASM v1.01 | Simple DoPIC16xx Cores dedicated assembler |

### DF6811, DF6808, DF6805 DoCD debugger

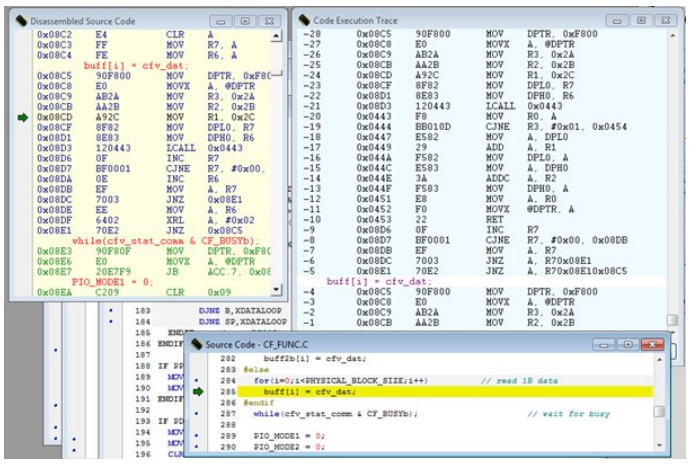
| File name | Description |
|---|---|
| 68xx DoCD v7.26 | DoCD™ DF6811 complete package |
| DF68xxdocd.dp | DoCD™ DF68xx datasheet |
| License | DoCD™ Software License Agreement |

## GO BEYOND THE LIMITS

System-on-Chip designs are facing the problem of inaccessibility of important control and bus signals, because they often lay behind the physical pins of the device – that makes traditional measurement instrumentation useless. The best way to get around those limitations, is to use on-chip debug tools for the tasks verification and software debuging. Other advantage of an on-chip debugger, is its improved design productivity in an integrated environment, with graphical user's interface. Ability to display/modify memories' content, processor's and peripherals' register windows, along with information tracing and ability to see the related C/ASM source code, are the key elements, that help to improve the design process and thereby, to increase productivity.

## INSTRUCTION SMART TRACE (IST)

The **DoCD™** Hardware Debugger provides debugging capability of a whole System on Chip (SoC). Unlike other on-chip debuggers, the DoCD™ provides non-intrusive debugging of a running application. It can also efficiently save designer's time, thanks to **hardware trace**, called **Instructions Smart Trace buffer (IST)**. The DoCD-IST **captures instructions in a smart and non-intrusive way**, so it doesn't capture addresses of all executed instructions, but only these related to the start of tracing, conditional jumps and interrupts. This method does not only **save time**, but also allows to **improve the size of the IST buffer and extend the trace history**. Captured instructions are read back by the DoCD-debug software, analyzed and then presented to the user as an ASM code and related C lines.



## PERFORMANCE

## PERFECT SERVICE FOR FREE

The reason for the developement of the **DoCD™**, was to provide our customers with the ability of easy system verification and software debugging, at no additional charges. Therefore, we have decided to add **the complete debug system** to each 8051/80251/80390 IP Core – **for free**

Now DCD's customers have the exceptional possibility, to obtain **the complete solution** for making their own 8051/80251/80390 based, SoC, with the ability to pre-silicon validation and post-silicon software debugging – **in one place**. It's really unusual opportunity for the designer, to have the ability to get a **high quality IP Core** and **unique on-chip debug tool**, from the same supplier.

## LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– ***Single-Site license option*** – dedicated to small and middle sized companies which run their business at one place.

– ***Multi-Site license option*** – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

– Verilog or VHDL RTL synthesizable source code (called HDL Source code)

– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

## CONTACT

**DCD-SEMI Headquarters:**
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd-semi.com
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
**Distributors:**
Please check: dcd-semi.com/contact-us/